SGS-THOMSON MICROELECTRONICS

L6254

SPINDLE

PRODUCT PREVIEW

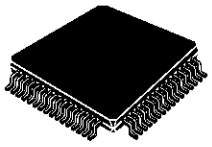
FEATURES:

Spindle Motor Driver

- Internal 4A peak current power drivers.
- Low Rds(on) 0.28 ohms maximum at 25°C.
- External current sense resistor.
- Slew rate control of both upper and lower drivers.
- Programmable linear or switch mode current driver.
- Constant off-time switch mode spindle power driver.
- Upper and lower drivers soft switching value externally set.
- Provide spindle active dynamic braking mode.
- Programmable spindle braking during power down condition.
- 15 KHz minimum spindle current control loop bandwidth.

Voice Coil Motor Driver and Retract Circuit

- Internal 2.5A peak current VCM power drivers.
- Low Rds(on) 0.4 ohms maximum at 25°C.
- External current sense resistor.
- External current control loop compensation.
- Zero dead-band and minimum cross over distortion.
- 20KHz minimum VCM current control loob bandwidth.
- Multi quadrant programmable retract down to 5 volts of BEMF.
- Constant hold voltage across the VCM down to 2 volts of BEMF.



TQFP64

ORDERING NUMBER: L6254

Power Monitor and Negative Voltage Regulator

- +5 volts and +12 volts power monitor threshold accuracy +/-2%.
- Hysteresis on both power monitor comparator.
- Precision internal voltage generator +/-2%.
- Buffered reference voltage output pin.
- Thermal sense circuit and an over temperature shut down.
- Internal booster voltage generator.
- Internal constant frequency switch mode voltage regulator for a negative power supply.

GENERAL DESCRIPTION

L6254 is a mixed signal ASIC that includes spindle motor driver, voice coil motor driver, retract circuit, brake circuit, power monitor and a negative voltage power supply voltage regulator.

The L6254 IC (Figure 1) is packaged in a 64 pin TQFP with Metal Slug for improved dissipation.

PIN DESCRIPTION

Power Monitor and Negative Voltage Regulator Circuit.

Number	Signal Name	Type	Functional Description
11	VCC5	IP	+5V power supply.
07	VCC12	IP	+12V power supply.
12	AGNDB	IP	Analog ground.
06	BSTCP1	OA	Booster input capacitor terminal 1.
09	BSTCP2	IA	Booster input capacitor terminal 2.
10	BSTFLT	OA	Charge pump booster output capacitor.
23	CPOR	IA	A capacitor is placed on this pin to program the power on reset delay.
20	NPOR	OD	Power on reset active low logic signal.
58	VPCNTRL	IZ	VCM driver enable mode of operation control. With the aid of an internal resistor divider VPCNTRL delivers three logic states. L = retract, H = enable, Z = disable. When V_{CC12} is connected to this pin the serial interface mode is enabled.
05	VSRET	IA	Reservoir capacitor is placed here to provide retract control voltage during BRAKE.
04	NVGD	IA	Negative voltage regulator external PFET gate control voltage.
02	VNVADJ	OA	Negative voltage regulator error amplifier output.
03	NVIS	IA	Negative voltage regulator error amplifier summing junction.
36	BRAKE	IA	Spindle brake activation threshold during power loss.
16	VREFOUT	OA	An internal 4V voltage reference buffered output.

Spindle Circuit.

Number	Signal Name	Type	Functional Description
61	SDRVU1	OA	Spindle motor coil terminal phase U.
62	SDRVU2	OA	Spindle motor coil terminal phase U.
56	SDRVV1	OA	Spindle motor coil terminal phase V.
57	SDRVV2	OA	Spindle motor coil terminal phase V.
52	SDRVW1	OA	Spindle motor coil terminal phase W.
51	SDRVW2	OA	Spindle motor coil terminal phase W.
64	VRET1	IA	3 phase power driver bridge input power. During power failure condition this pin provide the full wave rectified spindle BEMF voltage.
01	VRET2	IA	3 phase power driver bridge input power. During power failure condition this pin provide the full wave rectified spindle BEMF voltage.
53	VRET3	IA	3 phase power driver bridge input power. During power failure condition this pin provide the full wave rectified spindle BEMF voltage.
54	VRET4	IA	3 phase power driver bridge input power. During power failure condition this pin provide the full wave rectified spindle BEMF voltage.
59	SISINK1	OA	3 phase power driver bridge sink output.
60	SISINK2	OA	3 phase power driver bridge sink output.
49	SISINK3	OA	3 phase power driver bridge sink output.
48	SISINK4	OA	3 phase power driver bridge sink output.
43	SISENH	IA	External current sense resistor terminal. The other terminal of the current sense resistor must be connected to AGNDA.
42	AGNDA	IP	Analog ground.
55	SWPWR	OA	High voltage external power isolation NFET transistor gate control.

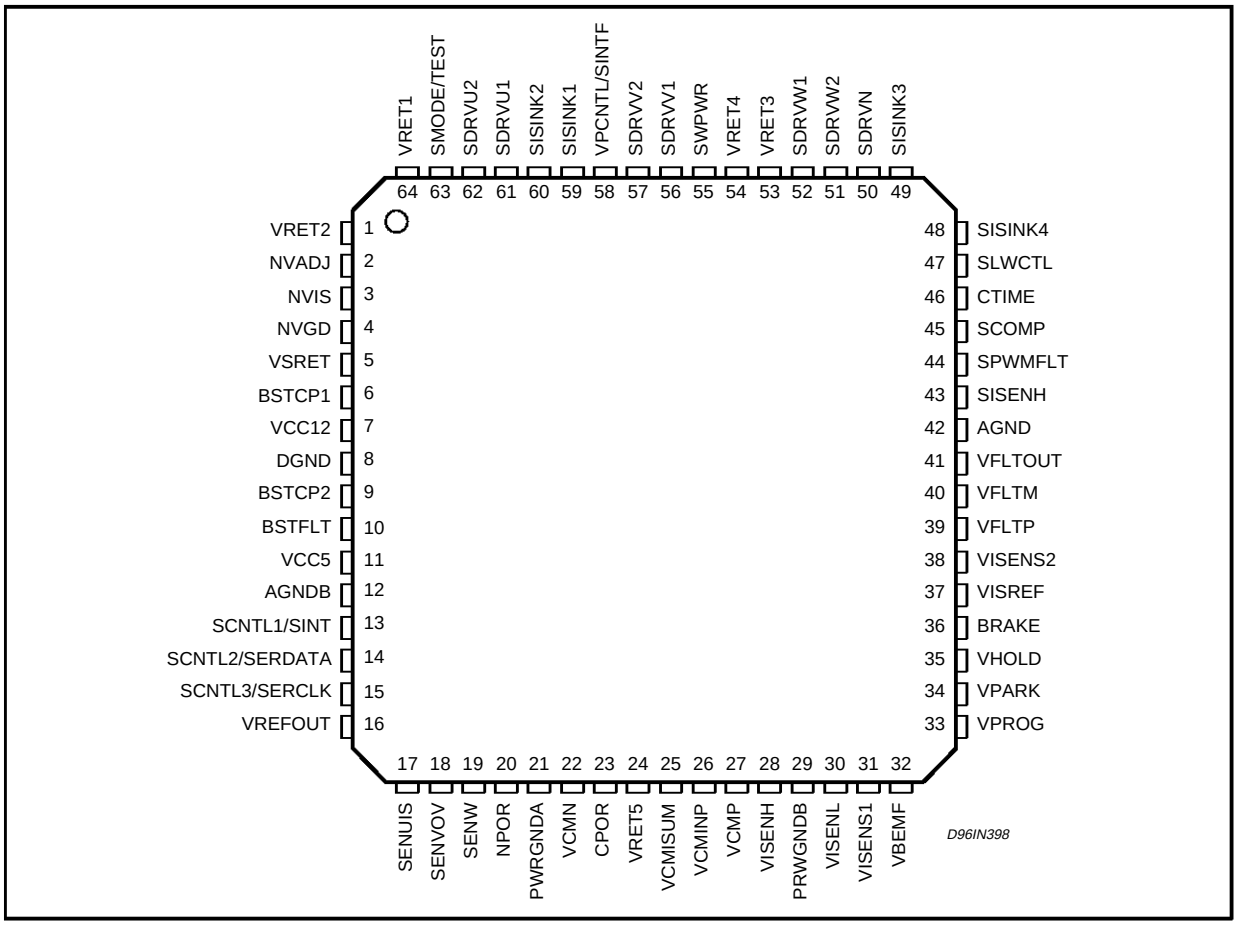
PIN DESCRIPTION (continued)
Spindle Circuit (continued)

Number	Signal Name	Type	Functional Description
50	SDRVN	IA	Spindle motor center tap.
13	SCNTL1/SINT	I/OD	Spindle state control bit 0 in the parallel interface mode and muxed BEMF comparator output in the serial interface mode.
14	SCNTL2/ SERDATA	I/O D	Spindle state control bit 1 in the parallel interface mode and serial data input/output in the serial interface mode.
15	SCNTL3/ SERCLK	ID	Spindle state control bit 2 in the parallel interface mode and the serial interface clock input in the serial interface mode.
8	DGND	IA	Digital ground.
17	SENUIS	OD	Spindle motor phase U BEMF comparator output or current comparator output controlled by the SMODE pin.
18	SENVOV	OD	Spindle motor phase V comparator output or VCM offset voltage comparator controlled by the SMODE pin.
19	SENW	OD	Spindle motor phase W BEMF comparator output.
63	SMODE/TEST	IZ	Spindle driver mode control. H == BEMF sense & Linear control. Z == Inductance sense & Linear control. L == BEMF sense & PWM control.. When V_{CC12} is connected to this pin test mode is enabled.
44	SPWMFLT	IA	Spindle motor current command analog input.
46	CTIME	IA	A capacitor is placed here to limit the on time during switch mode operation.
45	SCOMP	OA	Spindle current control loop compensation.
47	SLWCTL/ SSTOFF	OA	Slew rate programming for the H bridge upper and lower drivers.

Voice Coil Motor Driver and Retract Circuit.

Number	Signal Name	Type	Functional Description
39	VFLTP	IA	VCM current command active filter OP AMP plus terminal.
40	VFLTM	OA	VCM current command active filter OP AMP minus terminal.
41	VFLTOUT	OA	VCM current command filtered output.
25	VCMISUM	IA	The current control loop error operational amplifier summing junction.
26	VCMINP	OA	The current control loop error operational amplifier output.
28	VISENH	IA	VCM current sense amplifier input voltage non-inverting side.
30	VISENL	IA	VCM current sense amplifier input voltage inverting side.
31	VISENS1	OA	VCM current sense amplifier output 1. [Output is around VREFOUT level].
38	VISENS2	OA	VCM current sense amplifier output 2. [Output around VRET/2].
37	VISREF	IA	Reference voltage to set the zero current level of the second current sense amplifier.
27	VCMP	OA	VCM H bridge power driver output non-inverting coil terminal.
22	VCMN	OA	VCM H bridge power driver output inverting coil terminal.
24	VRET5	OA	VCM power driver H bridge input power.
21	PWRGNDA	OA	VCM power driver ground return.
29	PWRGNDB	OA	VCM power driver ground return.
35	VHOLD	IA	Hold mode programming current.
34	VPARK	IA	Park circuit programming voltage during four quadrant retract.
33	VPROG	IA	VCM control voltage during four quadrant retract.
32	VBEMF	OA	VCM back EMF voltage sense during retract. [Output is around VRET/2]

Figure 1: Pin connection.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_j	Junction Temperature	+150	°C
	Power Supply Voltage Vcc12	-0.3 to 15	V
	Power Supply Voltage Vcc5	-0.3 to 7	V
T_{stg}	Storage temperature	-55 to +150	°C
	Digital input voltage pins	-0.3V to Vcc5 +0.5	
	Analog input voltage pins	-0.3V to Vcc12 +0.5	
	BSTFLT pin	-0.3 to 24	V
	DC output current SDRVU-W	4	A
	DC output current VCMN-P	2.5	A
	ESD rating (all pins)	2000	V
	Latch up rating (all pins)	200 or Absolute Max. Volt.	mA
	Total power dissipation T_{amb} = 70°C	TBD	

CAUTION: Devices can suffer permanent damage and or reliability degradation if operated beyond the following maximum rating.

ELECTRICAL CHARACTERISTICS (The following specifications apply over the recommended operating ambient temperature range T_{amb} = 0 to 70°C and the recommended power supplies operating voltage range of V_{CC5}= 5 V -5% +10% & V_{CC12}= 12 V +/-10% unless otherwise specified)

Power Monitor and Negative Voltage Regulator

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
POWER SUPPLY CURRENT (Vcc5 & Vcc12)						
Icc5	+5V Supply current	Normal mode Sleep mode		7 7		mA mA
Icc12	+12V Supply current.	Normal mode Sleep mode		21 11		mA mA
VOLTAGE REFERENCE (VREFOUT)						
Vref	Voltage at VREFOUT	Rload > 400Ω Cload < 0.1µF	3.92	4	4.08	V
Irefouh	Source current		10			mA
Irefoul	Sink current		1			mA
PSRR	Power supply rejection ratio	f < 10kHz, ripple < 0.3V	50			dB
L_{REG}	Load Regulation	V_{REFOUT} = 4V I_{OUT} = 0 to 10mA			0.5%	$\%V_{OUT}$
VOLTAGE BOOSTER (BSTCP1 BSTCP2 BSTFLT)						
Vcp	Change pump voltage	Vcc12 = 10.8:13.2V	18		24	V
Iint	Internal load current				950	µA
Iload	Max. external load.	Vcp = Vcp initial - 0.2V			1	mA
	Short circuit output current	pin BSTFL			300	mA
AUXILIARY RETRACT POWER SUPPLY (VSRET)						
$I_{leakage}$	Leakage current at VSRET				100	nA
POWER MONITOR COMPARATORS						
Vt5	+5V Threshold voltage		TBD	4.625	TBD	V
Hv5	Hysteresis on Vcc5 comp.		50	75	100	mV
Vt12	+12V Threshold voltage.		9.7	10.10	10.50	V
Hv12	Hystetesis on Vcc12 comp.		100	140	180	mV
POWER ON RESET GENERATOR (CPOR AND NPOR)						
Icpor	CPOR charge current		2		4	µA
Vtpor	Trigger voltage	Vcc5 = +5V	2.2	2.5	2.8	V
Tpfmin	Power fault time that trigger POR.		8		20	µs
Vlow	NPOR low level voltage	Isink = 2mA			0.4	V
Vhigh	NPOR high level voltage		3.5			V
ttr	NPOR transition time	cload = 50pF			30	ns
OVER TEMPERATURE PROTECTION						
Twam	Thermal warming temperature	guaranteed by design	130	140	150	°C
Tsoft	Switch off temperature		150	160	170	°C
Thyst	Thermal Hysteresis		20		30	°C
NEGATIVE VOLTAGE REGULATOR OPAMP (NVIS, NVADJ)						
	Gain			60		dB
	Bandwidth			1		MHz
	Input offset			3		mV
	Input bias			1	2	µA
NEGATIVE VOLTAGE REGULATOR COMPARATOR (NVGD)						
	Hysteresis			60		mV
	Output swing		0		12	V
	Output transition	C_L = 600pF		150		ns
Voff	Output voltage during NPOR active		Vcc12			V

ELECTRICAL CHARACTERISTICS (continued)
Power Monitor and Negative Voltage Regulator (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
NEGATIVE VOLTAGE REGULATOR OSCILLATOR						
	Output swing		1.2		4.8	V
	Frequency			260		kHz

Spindle Motor Driver.

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SPINDLE POWER SWITCH (SWPWR)						
VoL	Low level output voltage	Isink = 1mA			1	V
VoH	High level output voltage		18			V
Tdhl	Output voltage high to low delay time from NPOR	Cload = 500pF 50% NPOR to Vout = 1V			1	µs
Iswp	Charge current	Cload = 500pF			9	µA
SPINDLE DRIVER MODE CONTROL (SMODE)						
Vh12	Voltage level for transition to test mode.	Vcc5 = 5V Vcc12 = 12V	7		9	V
Vh5	Voltage level for BEMF sense in linear mode.		3.75		5	V
Vts	Voltage level for induct. sense in linear mode.		2.25	2.5	2.75	V
V1	Voltage level for BEMF sense in PWM mode.				1.25	V
Rints	Input resistance.		7.5		50	kΩ
ttr	Input rise and fall time.	10%-90% Vcc5			20	ns
SPINDLE STATE CONTROL INPUTS (SCNTL1, SCNTL2, SCNTL3)						
Vh	High level input voltage	CMOS LEVEL	3.5			V
Vl	Low level input voltage				1.5	V
Iin	Input current		-10		10	µA
BACK EMF COMPARATORS (SENU, SENVOV, SENWIS)						
Vie	Common mode input voltage		0		12	V
Vr	Input voltage range where output shall not invert.		-1		15	V
Voe	Input offset voltage		-4		4	mV
Vhe	Hysteresis		2		10	mV
Vol	Low level output voltage	Iout = -1mA			0.5	V
Voh	High level output voltage	Iout = 1mA	3.5			V
SPINDLE OUTPUT DRIVERS (SDRVU, SDRVV, SDRVW)						
Rds(on)	Total output ON resistance (Source + Sink)	Iout = -1mA			0.28	Ω
		at 125°C			TBD	Ω
Idsx	Output leakage current	Idsx		1		mA
Vclmp	Clamp diode forward voltage	if = 1.0A			1	V
Icros	Current spikes during switching high or low side driver.	in PWM mode (guaranteed by design)				mA
CURRENT SENSE AMPLIFIER (SISENH)						
Virange	Current sense amplifier input voltage range		0		1.2	V
Gscs	Current sense amplifier gain	Measured in test mode.	5.82	6	6.18	
BW	Current sense amplifier unity gain bandwidth.	Guaranteed by design	1.5			MHz
Iin	Input bias current				1	µA
Vofs	Input offset		1	5.5	10	mV

ELECTRICAL CHARACTERISTICS (continued)
Spindle Motor Driver. (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
CURRENT SENSE COMPARATOR (SENIUS)						
	Hysteresis		48	60	72	mV
	Input offset voltage		-6		6	mV
	Response time				400	ns
CURRENT CONTROL LOOP COMPENSATION (SCOMP)						
gm	OTA amplifier transconductance gain		485	768	823	µA/V
Ccmp1 Ccmp2 Rcmp	External network at SCOMP			TBD TBD TBD		nF nF kΩ
Gsi	Transconductance gain: Iout / SPWMFLT input pin.	Rsense range = Rs (0.12 to 0.4)Ω	-4%	1/6Rs	4%	A/V
	Gain linearity error	Vin = 0.1 to 0.9 Vref	-1		1	%
	Voltage at SPWMFLT to command zero output current.	Imotor = 0	0		80	mV
	Operating voltage range at SPWMFLT		0		5	V
	Maximum motor current.	SPWMFLT = Vref	0.65/Rs			A
	Current loop bandwidth from SPWMFLT	Guaranteed by design	15			kHz
IiSPWM	Input bias current SPWMFLT				-3	µA
	Power supply rejection ratio	f < 10kHz, rip. < 0.3V Imotor > 0.2A	60			dB
OUTPUT DRIVERS SLEW CONTROL (SLWCTL)						
Rslew	External resistor at SWCTL		TBD	100	TBD	kΩ
SRhon	SDRV_X output voltage slew rate during switching high side driver on in linear mode or switching high driver on or off in switch mode.	Lm = 0.3mH R_{Load} = 1.2Ω	TBD	10	TBD	V/µs
SRhoff	SDRV_X output voltage slew rate during switching high driver off in linear mode.	Lm = 0.3mH R_{Load} = 1.2Ω Rslew = 100k	TBD	0.3	TBD	V/ms
			TBD	0.3	TBD	V/µs
	SDRV_X output voltage slew rate during switching low side driver off in linear mode.					
SRloff	SDRV_X output voltage slew rate during switching low side driver on in linear mode.		TBD	1.2	TBD	V/µs
SRlsw	SDRV_X output voltage slew rate during switching low side driver on or off in linear mode.	Lm = 0.3mH R_{Load} = 1.2Ω	TBD	10	TBD	V/ms
PWM TIMING (CTIME, SLWCTL)						
voffl	Toff low threshold	pin SLWCTL Vcc5 = 5		1.25		V
voffh	Toff high threshold			2.5		V
Ichar	Charge current	pin CTIME		20		µA
Vthl	Low voltage threshold		(Vcc5/2) - Vthp			V
Vthh	Hi voltage threshold		(Vcc5/2) - Vthn			V
Vhys	Hysteresis		Vthp + Vthn			V
SPINDLE BRAKE PROGRAMMING (BRAKE)						
Vbrake	Brake threshold voltage at Vref 1, 2, 3, 4 and 5.	R_{VRET} = 15K, R_{GND} = 5K R_{VRET} = 50K, R_{GND} = 5K	1.3 3.9		1.5 4.3	V V

ELECTRICAL CHARACTERISTICS (continued)
Voice Coil Motor Driver

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VCM CURRENT COMMAND FILTER SALLEN KEY FILTER BUFFER (VFLTP, VFLTM)						
	Common mode input voltage range.		0		Vref	V
Avg	Voltage gain.		80			dB
BW	Unity gain bandwith.	Cload = 50pF	4			MHz
Cload	Maximum load capacitance.			TBD		pF
SR	Output slew rate.		2			V/µs
Io	Maximum output current		1			mA
Ibias	Input bias current.				500	nA
Vio	Input offset voltage.		-3		3	mV
PSRR	Power supply rejection ratio.	f < 10kHz, rip. < 0.3V	60			dB
Vout	Output voltage swing	Iout = 1mA	0		Vref	V
VCM CURRENT COMMAND LEVEL SHIFTER (VFLTM, VFLTOUT)						
	Common mode input voltage range.		0		Vref	V
Avg	Voltage gain.		80			dB
BW	Unity gain bandwidth	Cload = 50pF	2			MHz
Cload	Maximum load capacitance.			TBD		pF
SR	Output slew rate.		2			V/µs
Io	Maximum output current		1			mA
Ibias	Input bias current.				500	nA
Vio	Input offset voltage.		-3		3	mV
PSRR	Power supply rejection ratio.	f < 10kHz, rip. < 0.3V	60			dB
Vout	Output voltage swing	Iout = TBD	Vret/2 – Vref/2		Vret/2 + Vref/2	V
CURRENT SENSE AMPLIFIERS (VISENL, VISENH, VISENS1, VISENS2)						
Rin	Input resistance VISENL to VISENH.		3			kΩ
Vts	Common mode input voltage range.		-0.5		Vcc12+ 0.5	V
Vof	Input offset voltage		-4		4	mV
	Bias current	VISREF = 5V			1	µA
	Output load VISENS1.				50	pF
	Output load VISENS2.				150	pF
	GAIN1	(VISENSE1 -VREFINT) / (VISENH - VISENL)	7.8	8	8.2	
	GAIN2	(VISENS2 - VISREF) / (VSENH - VISENL)	2.4	2.5	2.6	
Vouts 1	Output voltage swing SENSE1.	R1 = 10kΩ	2		10	V
Vouts2	Output voltage swing SENSE2.		0.5		5	V
	Output slew rate SENSE1.		1			V/µs
	Output slew rate SENSE2.		0.5			V/µs
	Unity gain BW SENS1.		2			MHz
	Unity gain BW SENS2.		1			MHz
CMRR	Common mode rejection ratio.	f < 10kHz, rip < 0.3V	60			dB
PSRR	Power supply rejection ratio	f < 10kHz, rip < 0.3V	60			dB

ELECTRICAL CHARACTERISTICS (continued)
Voice Coil Motor Driver (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
ERROR SUMMING AMPLIFIER (VCMISUM, VCMINP)						
Avg	Voltage gain.		80			dB
	Unity Gain Bandwidth		2			MHz
Cload	Maximum Load Capacitance				50	pF
SR	Output Slew Rate		1			V/µs
Io	Output current.		1			mA
Ibias	Input bias current				500	nA
Vio	Input offset voltage		-4		4	mV
PSRR	Power supply rejection ratio.	f < 10kHz, rip. < 0.3V	60			dB
Vclamp	Voltage clamp across VCMISUM and VCMIN		±1.5		±2.4	V
Vout	Output voltage swing	Iout = max out current	Vret/2 – Vclamp		Vret/2 – Vclamp	V
VCM OFFSET COMPARATOR (SENVOV)						
	Hysteresis			0		mV
	Input offset voltage		-6		6	mV
	Response time				400	ns
	Common mode input voltage range.		2		10	V
VCM OUTPUT DRIVERS (VCMP, VCMN)						
Rds(on)	Total output ON resistance (Source + Sink)	Iout = 1 at 25°C Iout = 1 at 125°C			0.4 TBD	Ω Ω
Idsx	Output leakage current				100	µA
Eln	Linearity error of output drivers	Vout = 0: 10V			TBD	%
Sym	Output symmetry error [(vcmx/vcmy) - 1] x 100.	Iout = ±100mA			TBD	V
	Clamp diode forward voltage	If = 1A			TBD	V
Gdpoa	Power operational amplifier differential gain.		15	16	17	V/V
	Zero crossing distortion for a 90Hz 50mA sine wave current	Guaranteed by design. Characterized only, not tested.			1	µs
	Total harmonic distortion	Iout = ±100 mA Guaranteed by design. Characterized only, not tested.			TBD	%
SR_{VCM}	Output VCMN or VCMP slew rate during fast switching	L_M = 0mH R_L = 10.0Ω		3		V/µs
VCM CURRENT CONTROL LOOP STATIC AND DYNAMIC CHARACTERISTIC						
Givcm	Transconductance gain: Iout / Vinput at VFLTOUT.	Rsense, R1, R2, R3, C1 see figure (TBD)	TBD		TBD	A/V
	Gain linearity error from: VFLTOUT to output current	Vin = 0.1:0.9Vref	-1		1	%
Vto	Total offset current	VFLTOUT = Vref/2			TBD	mA
	Open loop bandwidth from: VCMINP to Output current		100			kHz
	Current control loop bandwidth from VFLTOUT to motor current		25			kHz

ELECTRICAL CHARACTERISTICS (continued)
Voice Coil Motor Driver (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VCM AND RETRACT CONTROL (VPCNTL)						
Vh12	Voltage level for transition to serial interface.	Vcc5 = 5V Vcc12 = 12V	7		9	V
Vh5	Voltage level for VCM enable		3.75		5	V
Vts	Voltage level for VCM disable		2.25	2.5	2.75	V
Vl	Voltage level for VCM retract.				1.25	V
Rints	Input resistance		7.5		50	kΩ
ttr	Input rise and fall time	10%-90% Vcc5			20	ns
VCM RETRACT PROGRAMMING AND CONTROL (VBEMF, VPROG, VPARK, HOLD)						
Gdiff	VBEMF amp. dif. gain.		0.118	0.125	0.131	V/V
SR	VBEMF amplifier output slew rate.	Rload = 1kΩ Cload = 1µF	0.01			V/µs
CMRR	VBEMF amplifier common mode rejection ratio	F < 10kHz, rip. < 0.3V	18			dB
Rdsonr	Total on resistance during retract.				4	Ω
Tprog	Time delay between the end of flyback and O/P stage enable			170		µs
	Input bias current of retract power drive amplifier				500	nA
	Retract hold current after retract stage drop out		50		100	mA
Vpark	VRET voltage for parking		4.8			V
Vhold	VRET voltage for holding		2		4.8	V
Ih	Hold voltage progr. curr.				100	µA
Vhr	Voltage on load during holding.	meas. between GND and VCMP or VCMPN	0.1		1	V

Spindle VCM Cross Channel Interference

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
INTFsv	Spindle channel interference from the VCM channel	Ivcm = ±1.5A Ispindle = 0.25A			-60	dB
INTFvs	VCM channel interference from the Spindle channel	Ivcm = ±0.2A Ispindle = 0.9A			-60	dB

Serial Port

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{pd}	Internal pull down resistor		TBD	20	TBD	kΩ
t_{isetup}	SERDATA input setup to clock required.		20			ns
t_{ihold}	SERDATA input hold after clock required		10			ns
t_{odly}	Clock to SERDATA output propagation delay	C_L = 30pF R_L = 20k	0	10	20	ns
	Clock to SERDATA output hi-Z delay	C_L = 30pF R_L = Rpd	0	10	20	ns
	Clock to SERDATA output low-Z		0	10	20	ns

Interface Description

The L6254 IC is designed to interface to a custom digital ASIC which provides the L6254 IC with the necessary control signals and complement its motor driver function. The L6254 IC and the custom ASIC can be connected via a serial or parallel interface.

Parallel Interface

In the parallel interface configuration the SMODE signal controls the mode of operation of the spindle motor driver, while SCNTL1, SCNTL2 and SCNTL3 provide the spindle driver with the commutation sequence. The SENUIS, SENVOV, SENW signals furnish the digital ASIC with the needed back EMF feedback to commutate the driver. The VPCNTL signal controls the VCM driver mode of operation. Figure 2 shows the parallel interface configuration between L6254 and a custom ASIC in a typical application circuit.

Serial Interface

In the serial interface configuration the L6254 serial port is enabled by connecting VPCNTL pin to VCC12. The input pins SERDATA, SERCLK and SINT are used to write and read data from the L6254 IC. An internal control register provides the spindle mode control, the spindle commutation sequence and the VCM mode control. The spindle back EMF feedback can be recovered by reading the status register or use the multiplexed back EMF comparators output on the SINT pin.

The L6254 serial port are also used during testing to program other internal functions. Figure 3 shows the serial interface configuration between L6254 and a custom ASIC in a typical application circuit. The L6254 test mode is enabled by connecting SMODE pin to VCC12.

Figure 2: L6254 IC Parallel Interface Typical Application.

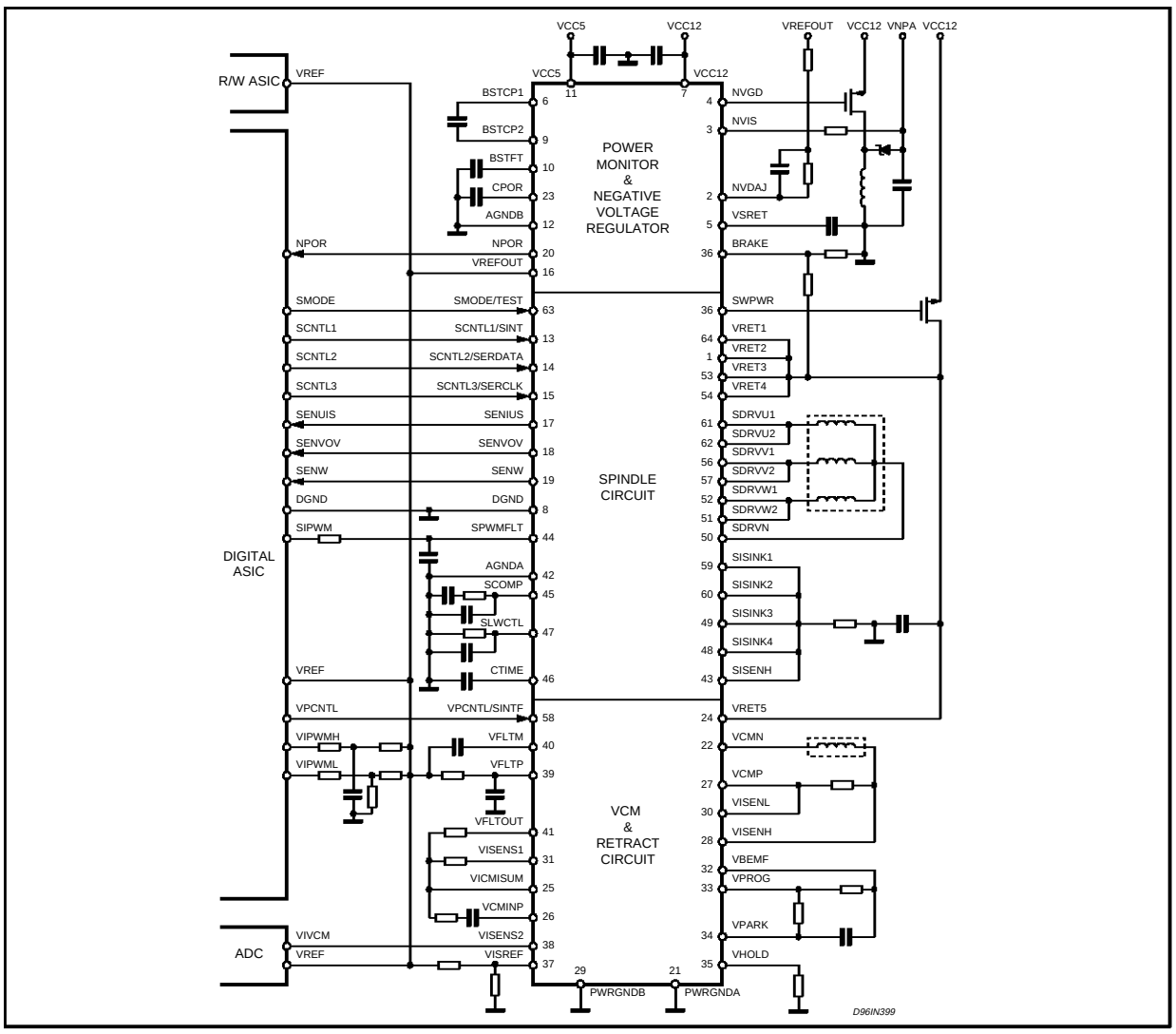
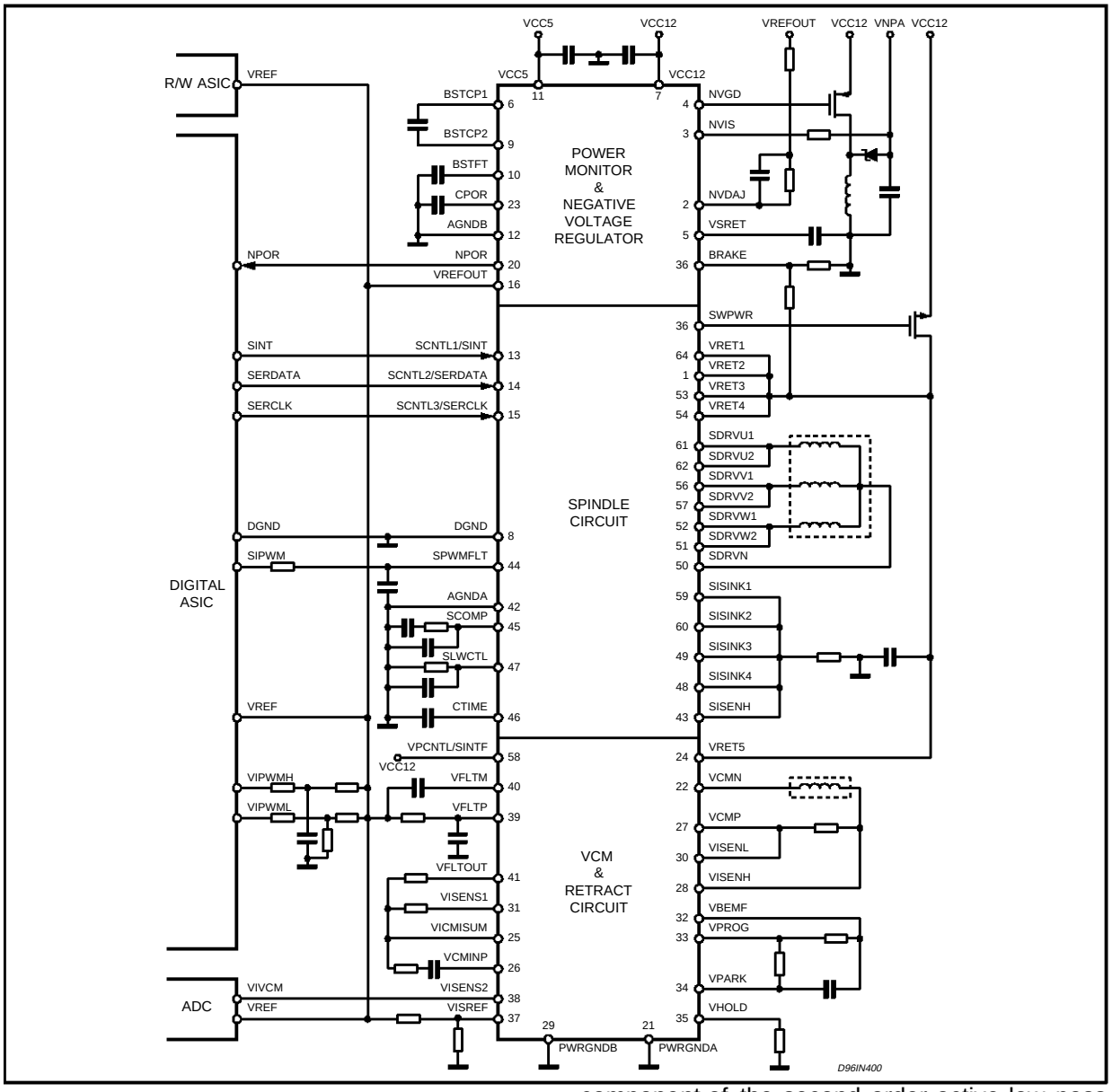


Figure 3: L6254 IC Serial Interface Typical Application.



Spindle Current Command Description

The spindle motor driver current is programmed from an 8 bit resolution single bit PWM DAC located inside the custom ASIC. The DAC output is filtered externally and then applied as an analog voltage at the L6254 IC SPWMFLT input pin.

VCM Current Command Description

The VCM driver current is programmed from a 14 bit resolution two bit PWM DAC located inside the custom ASIC. The DAC outputs VIPWMH and VIPWML are summed and filtered by an external third order filter. An internal operational amplifier designed in the L6254 IC serves as the active component of the second order active low pass filter stage. The VCM filtered motor current command is the L6254 IC operational amplifier output pin VFLTOUT.

VCM Current Sense Description

The VCM current is differentially sensed, amplified and level shifted to VRET/2 voltage level by a differential amplifier on the L6254 IC. The VCM current sense output is available at VSENS1 output pin. An additional VCM current sense output which is level shifted to VISREF input voltage is also available at the VISENS2 output pin. The VISENS2 is dedicated to the external analog to digital converter VCM current channel input.

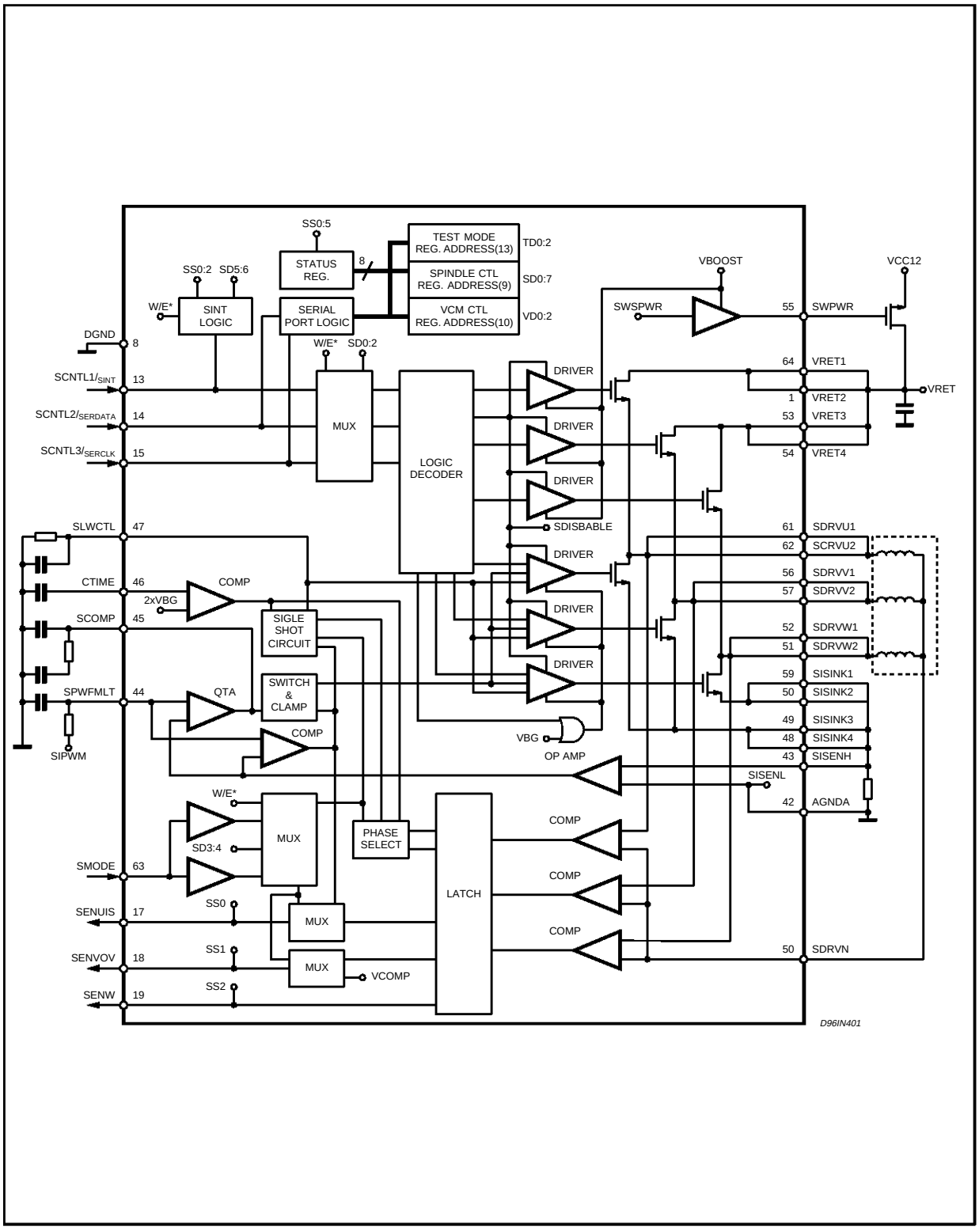
FUNCTIONAL DESCRIPTION

SPINDLE MOTOR DRIVER

The spindle motor driver block diagram is shown in Figure 4.

A brief function description of its different parts are as follows:

Figure 4: L6254 Spindle Circuit Block Diagram.



Spindle Motor Driver Operating Modes and Control

The spindle motor driver mode of operation is controlled by a triple level logic signal SMODE pin 63 in the parallel application as follows:

1) Level tri_level [V_{cc5}/2] place the driver in inductance sense mode.
2) Level low [0V] place the driver in switch mode current control.
3) Level high [5V] place the driver in linear mode current control.

In the serial application bits 3, 4 of the Spindle Control Register control the spindle mode of operation. Review bit definitions on page 18.

INDUCTANCE SENSE MODE

During the spindle motor start up the inductance sense mode is used to find the rotor position. The spindle BEMF comparator phase U output is switched to the current sense verses input current command comparator output. The disk drive system controller evaluate the rotor position by exciting each phase separately for a short period of time, then compare the rise time for each phase with the average rise time.

SWITCH MODE CURRENT CONTROL

In the switch mode current control operation only the high side drivers are pulse width modulated to control the current in the motor. The low side drivers are fully switched on or off according to their commutation sequence timing. The PWM control of the high side drivers is achieved by a constant Toff single shot circuit. The timing of the single shot circuit can be programmed by an external capacitor at the SLWCTL pin 47. In the switch mode an internal high side driver slew rate limiter circuit is used to reduce the coil voltage spikes during switching. In addition a circuit is used to turn on the appropriate low side driver during switching off the high side driver providing a circulation path for the coil current. The current control is the switch mode is achieved by controlling the turn on of the high side driver selected by the commutation sequencer. The high side driver is kept in the on state till the current comparator toggles indicating that the current sense is equal to the commanded current. Then the single shot circuit is started and the high side driver is turned off. The process repeats after the single shot time expires. An added timing circuit is used to allow clocking the BEMF zero crossing data during startup. This circuit timing can be programmed by an external capacitor at CTIME pin 48.

LINEAR CONTROL MODE

In the linear mode the current control is achieved by using the integrated compensated difference between the current command and the current sense to modulate the gate source voltage of the low side driver phase selected by the commutation sequencer. The high side drivers are fully switched on or off according to their commutation sequence timing. A slew rate control of the low and high side drivers are provided to reduce the switching coil current transients. The slew rate value can be set externally by a resistor on the SLWCTL pin 47.

Spindle Power Driver H Bridge

The spindle power driver consists of a 3 phase H bridge power transistor. Both the low and the high side drivers are NMOS transistors. The drivers are built by a special low Rdson DMOS power structure. The 12 volts power supply is connected to the H bridge via an external power NMOS device. The H bridge returns to ground through the sink pins and via an external sense resistor. An on-chip Boost voltage generator is being used to switch the high side drivers and the external isolation NMOS.

Commutation Decoder

The spindle power driver commutation sequence are decoded from the three input control signals SCNTL1, SCNTL2 and SCNTL3 in parallel interface configuration of from the spindle control register bit 0:2 during serial interface operation according to Table 1. Figure 5 shows the timing relationship of the control signals, the spindle motor coil voltages and the expected BEMF comparators output.

Slew Rate Control

A Slew Rate Control circuit becomes active in the linear mode of operation. During turning off both the low and the high side driver the gate control voltage are slewed to control the rate of charge of the output current. The slew rate control is also active during turning on the low side drivers in the linear mode. The slew rate can be programmed by a resistor on the SLWCTL pin (47).

BEMF Sense Comparators

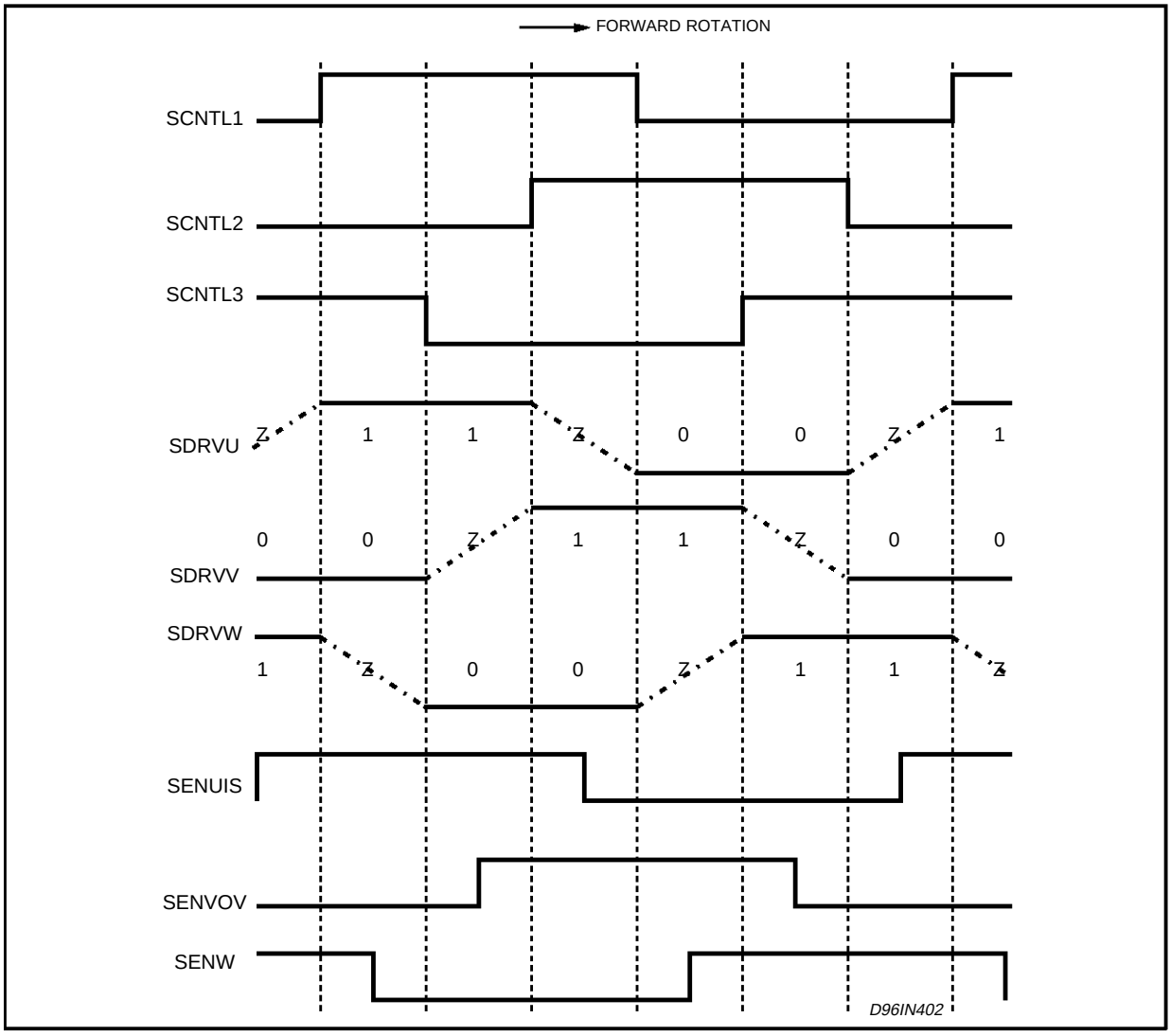
The spindle motor commutation timing are generated by an external ASIC which uses the unenergized motor phase BEMF zero crossing timing information as an input. The BEMF comparators are designed to accurately decode the BEMF zero crossing. A transparent latch are added on the comparators output to prevent the comparators from toggling due to switching noise while operating the driver in switch mode. During start up the C_{TIME} timing circuit allows clocking the BEMF zero crossing data while the high side driver is in the on state.

Table 1: Spindle Motor Commutation Sequence Decoder.

ENCODED STATE	CONTROL STATE			MOTOR WINDING STATE		
	SCNTL3	SCNTL2	SCNTL1	SDRVW	SDRVV	SDRVU
SPINDLE DISABLE	0	0	0	Z	Z	Z
STATE A	1	0	1	Z	0	1
STATE B	0	0	1	0	Z	1
STATE C	0	1	1	0	1	Z
STATE D	0	1	0	Z	1	0
STATE E	1	1	0	1	Z	0
STATE F	1	0	0	1	0	Z
DYNAMIC BRAKE	1	1	1	0	0	0

Notes:
1) The spindle motor driver control circuits are insensitive to the direction of motor rotation.
2) State 1 indicates switching on the high side driver, state 0 indicates switching on the low side driver and state Z indicates both low and high side driver are off.

Figure 5: L6254 Spindle Commutation Timing.



SERIAL INTERFACE

The L6254 serial interface is enabled by connecting the VPCNTL pin 58 to VCC12 power supply pin. An internal voltage comparator detects the VCC12 voltage level on VPCNTL pin, switch on the serial port logic and mux both the spindle and the VCM control signals and status to the serial port registers.

SERIAL PORT ARCHITECTURE

The serial port consists of the following two pins:

- SERCLK [serial interface clock] pin 15: Driven by an external master node.
- SERDATA [serial interface data] pin 14: Either driven by an external master node during write or by L6254 during read.

WRITE PROCESS

To write, the external master node turns on the SERDATA driver, outputs the start bit, shifts out the address, a 1 to indicate a write, a dummy bit, and then shifts out the 8 bits data to be written. The data output is followed by a cycle in which a trailing 0 is output. See Figure 6.

READ PROCESS

To read, the EXTERNAL master turns on the SERDATA driver, outputs the start bit, shifts out the address, and a 0 to indicate a read. It then tri-states SERDATA and invokes a dead cycle to allow time for the SERDATA driver to turn off before the slave driver is turned on. The next 9 clock cycles are used to shift in 8 bits of data from the slave and to allow the slave to drive a trailing 0 to actively pull SERDATA down before it is released. See Figure 6.

INITIALIZATION

To initialize the serial port, the external master node does the following:

1) Tri-states SERDATA and waits a while to let a passive pull down put a 0 on the wire
2) Tri-states the SERDATA and issues a minimum of 16 clocks to L6254, then
3) Drives a low onto SERDATA, and issued another minimum of 16 clocks.

Whenever L6254 sees 16 consecutive 0s clocked in, it resets the state of the serial port. The reset of the serial port only resets the serial port logic but does not clear the data registers.

Figure 6: Serial Port Data Packet Format.

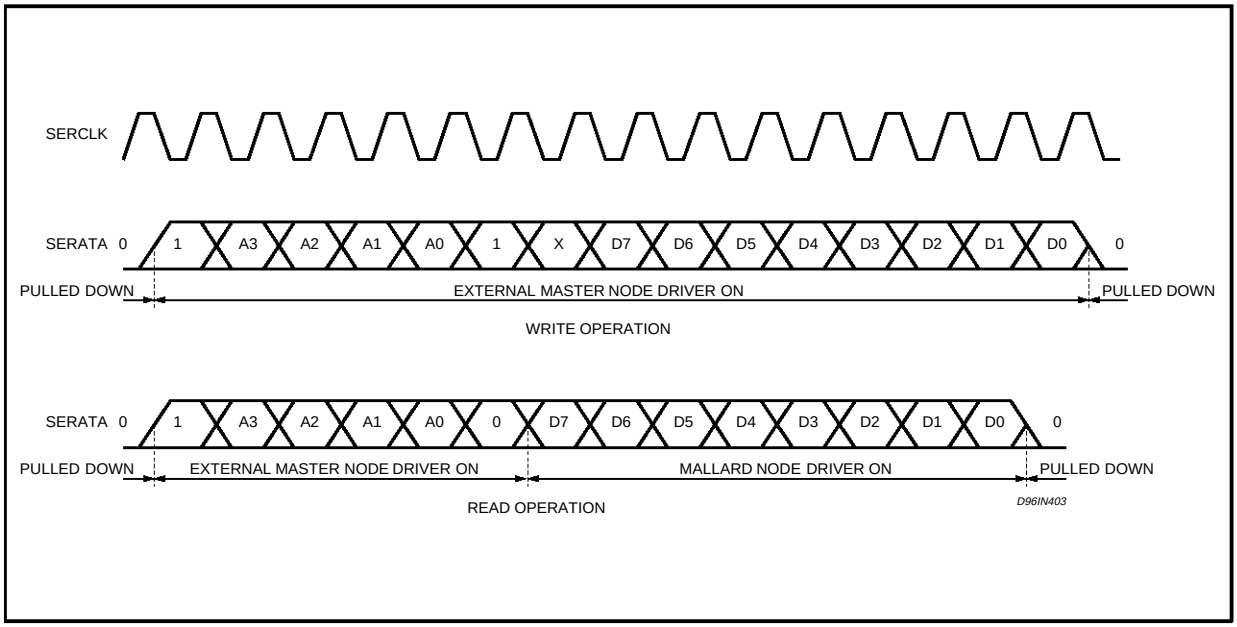
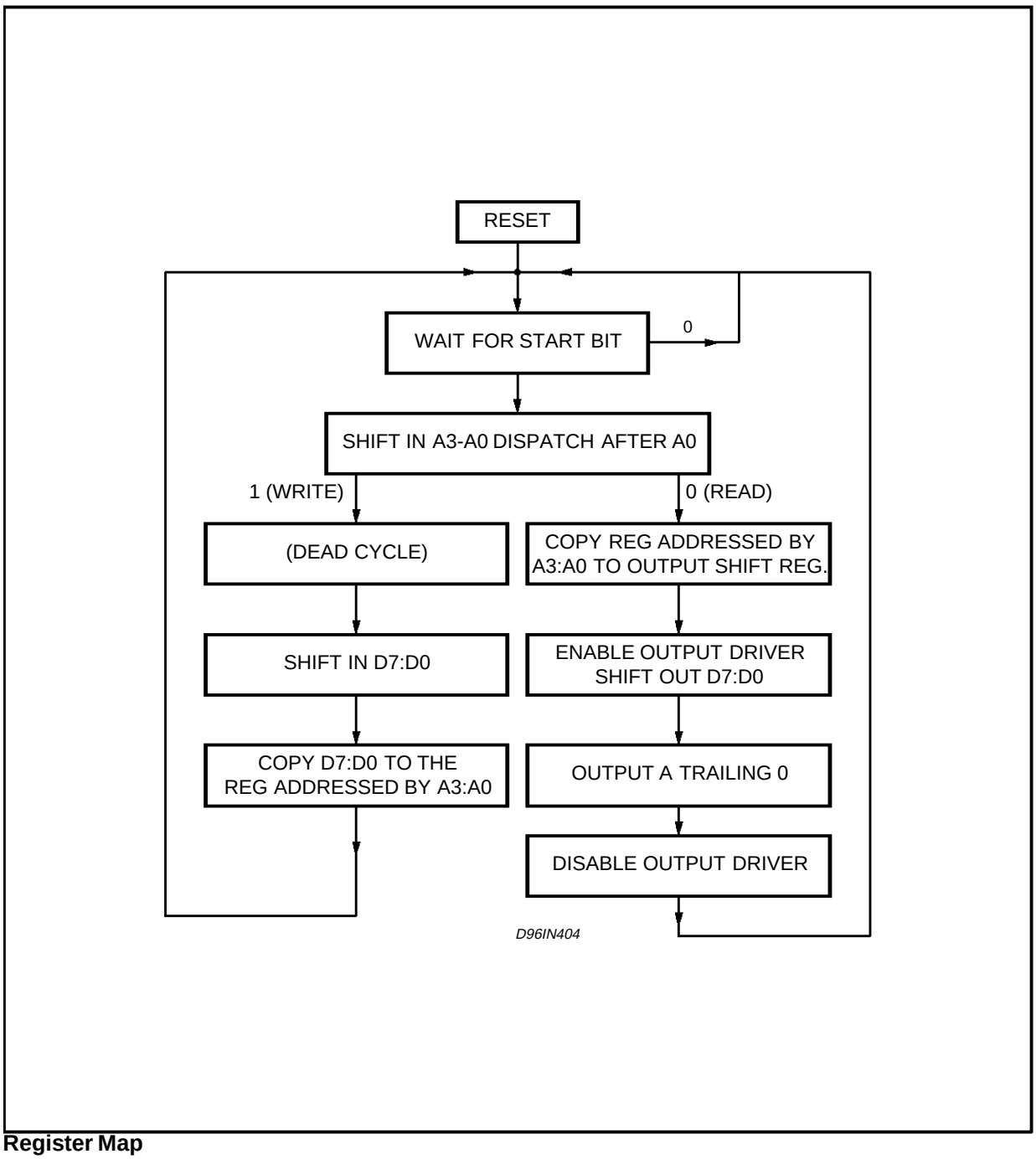


Figure 7: Serial Port State Flow Diagram..



Register Map

DATA REGISTERS

Table 2: REG - 07h STATUS REG: Miallard Status Register (Read Only)

R/O	7	6	5	4	3	2	1	0
	Reserved		VCOMP	OVER TEMP	OVER TEMP WARNING	SENW	SENVOV	SENUIS
	X	X	0	0	0	0	0	0

Bits 7 - 6: Reserved

Read as zeros.

Bit 5: VCOMP

The VCM offset comparator output.

Bit 4: OVER TEMP

This bit indicates that the junction temperature exceeded the maximum allowable temperature of 150°-170°C.

Bit 3: OVER TEMP WARNING

This bit indicates that the junction temperature exceeded 130°-150°C.

Bit 2: SENW

The spindle back EMF sense comparator output phase W.

Bit 1: SENVOV

The spindle back EMF sense comparator output phase V or the VCM offset comparator output during inductance sense mode.

Bit 0: SENUIS

The spindle back EMF sense comparator output phase U or the current comparator output during inductance sense mode.

Table 3: REG-09 SCREG: Spindle Control Register (Read/Write)

RD/WR:	6	5	4	3	2	1	0
	SENSEL1	SENSL0	BEMF/-IND SENSE	PWM/-LIN	SCNTL3	SCNTL2	SCNTL1
	1	1	0	0	0	0	0

This register is a read write register can be read at the same address. During power-on reset register is cleared to 60 Hex.

Bit 7: BEMF Latch Edge

When active the BEMF zero crossing data is latched when driver is turning on during switch mode of operation, otherwise is latched when driver is turning off during switch mode (default).

Bit 6: SENSEL1

High order bit in the select back EMF mux control for SINT line.

Bit 5: SENSEL0

Low order bit in the select back EMF mux control for SINT line.

SENSEL1 (BIT 6)	SENSEL (BIT 5)	SINT (PIN 13)
0	0	SENUIS
0	1	SENVOV
1	0	SENW
1	1	Exclusive NOR of (SENVIS & SENVOV & SENW)

Bit 4: BEMF/-IND SENSE

The spindle mode of operation BEMF sense or inductance sense select bit.

Bit 3: PWM/-LIN

The spindle driver mode of operation select bit, either switch mode or linear mode select bit.

Bit 2: SCNTL3

The spindle state control bits, bit three.

Bit 1: SCNTL2

The spindle state control bits, bit two.

Bit 0: SCNTL1

The spindle state control bits, bit one.

Table 4: REG -Ah: Voice Motor and Retract Register (Read/Write)

RD/WR:	7	6	5	4	3	2	1	0
	Reserved						-RETRACT	-DISABLE
	X	X	X	X	X	X	0	0

This register is read write register can be read at the same address. During power-on reset register is cleared to 00 Hex.

Bits 7 - 2: Reserved

Read as zeros.

Bit 1: - RETRACT

VCM driver retract enable bit negative true.

Bit 0: - DISABLE

VCM disable bit negative true.

SINT Line Pin 13

The optional signal SINT carries the spindle back EMF zero crossing timing information. During programming the spindle commutation state the serial port data either select a phase of the back EMF comparator output to the SINT line or select the exclusive nor function of the comparators output.

Table 4: REG -Dh: L6254 Test Control Register (Write Only)

W/O	7	6	5	4	3	2	1	0
	Reserved					TST2	TST1	TST0
	X	X	X	X	X			

TESTS	TST2	TST1	TST0	INTERNAL STATUS
NO TEST	0	0	0	
TEST 1	0	0	1	- bemfsns => buffer senuis - pwmin => buffer senv - testmod => buffer senw - disable buffer vret/2 — SMODE test
TEST 2	0	1	0	- serial => buffer senuis - venable => buffer senv - vretrac => buffer senw — VPCNTL test
TEST 3	0	1	1	- temphys => pin senuis - shunthres => pin senv - vrefout => pin senw - vret/2 => pin visref
TEST 4	1	0	0	- ctiout => pin senv - smout => buffer senw (Power Monitor Comparator) - senout => pin visref - enable VCM BEMF amplifier

Warning: Test mode is only intended for production testing. An attempt to use this mode during normal operation may result in permanent damage of the L6254 IC.

VOICE COIL MOTOR DRIVER

The VCM driver block diagram is shown in Figure 2-5. A brief function description of its different parts are as follows:

VCM Operating Modes and Control

In the parallel interface mode the VCM mode of operation is controlled by a triple level signal VPCNTL pin 58 in the parallel interface configuration as follows:

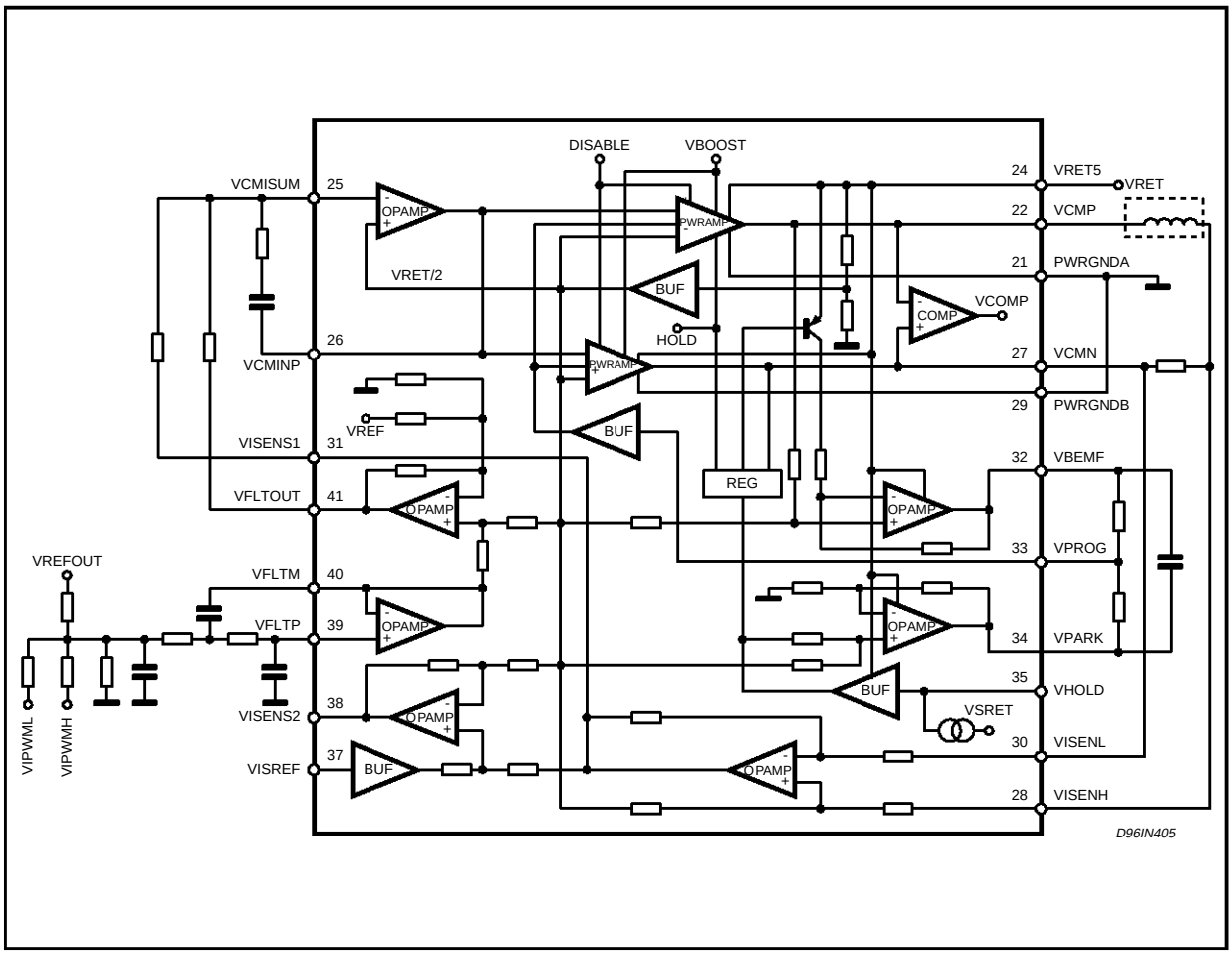
1) Level tri_level [V_{CC5}/2]. Disable VCM driver.
2) Level low [0V]. Place VCM driver in retract mode.
3) Level high [5V]. Enable the VCM driver.

In the serial interface mode the VCM two bits control register furnishes the VCM mode of operation as follows:

VD1	VD0	VCM Mode of Operation
Low	Low	Retract
Low	High	Retract
High	Low	Disable
High	High	Enable

During power-on-reset the VCM register is cleared and the VCM is in Retract mode of operation.

Figure 8: L6254 VCM and Retract Circuit Block Diagram.



VCM Power Driver H Bridge

The VCM is a high performance linear; class AB, H bridge type power driver with all power devices internal to L6254. The H bridge consists of 4 NMOS power transistors built by a special low rdson DMOS power structure. The power supply to the H bridge is connected via an external power transistor at V_{RET5} pin 24. The H bridge returns to ground via PWRGNDA pin 21 and PWRGNDB pin 29. The power amplifier differential gain is 16.

VCM Input Current Command

The L6254 provides an operational amplifier to buffer the VCM input current command from a DAC or to implement a PWM DAC filter with the operational amplifier being used as the active component of a second order active low pass filter in salen key configuration. The zero VCM input current request must correspond to $V_{REF}/2$ voltage level at the VFLTM pin 40. The PWM DAC filter configuration is shown in the VCM block diagram Figure 2-5. Following the operational amplifier is a level shifter which level shift the input current command from $V_{REF}/2$ to $V_{RET}/2$ voltage level. The output of the level shifter appears at the VFLTOUT pin 41.

VCM Current Sense

The VCM current sense is achieved by sensing the voltage drop across an external current sense resistor is series with the VCM coil. The L6254 current sense amplifier amplifies the differential voltage across its input terminals (VISENH pin 28 and VISENL pin 30) eight times and level shifts the amplified voltage to $V_{RET}/2$.

The output of the current sense amplifier is available at VISENS1 pin 31. An additional VCM current sense output is provided at VISENSE2 pin 38. The second current sense amplifier amplifies the voltage across VISENH and VISENSL by a gain factor of 2.5. visens2 is also level shifted to an arbitrary voltage level set by the VISREF input pin 37. The second VCM current sense output is intended for use as input to an external analog to digital converter.

VCM Current Loop Error Amplifier

The VCM current loop error amplifier serves as a summing amplifier which generates an output voltage proportional to the dynamically compensated voltage difference between the requested input voltage from VFLTOUT pin 41 and the actual motor current sense voltage VISENS1 pin 31. The dynamic compensation is achieved by an integrator and a lead network connected across the VCMISUM pin 25 and VCMINP pin 26. The integrator reduces the DC error to zero, while the lead network cancels the VCM electrical time constant.

The output of the VCM current loop error operational amplifier drives the power amplifier which in turn drives the VCM coil. The output of the error amplifier is level shifted to $V_{RET}/2$ via connecting its non-inverting input internally to $V_{RET}/2$.

A voltage limiter is connected on the error amplifier output to achieve the fast recovery needed when the output voltage changes direction with large voltage swing. The voltage limiter consists of 3 series forward biased diodes in parallel with 3 series reverse biased diodes which are internally connected across the amplifier output VCMINP pin 26 and its summing junction VCMISUM pin 25.

VCM Retract and Hold

During power on reset condition or when the microcontroller command retract is issued, the VCM retract and hold circuit is used to retract and park the voice coil actuator. The retract circuit consists of a fly back detect circuit, VCM BEMF sampling timing circuit, BEMF sampling amplifier, park voltage amplifier & level shifter, power amplifier programmable retract voltage buffer, hold level voltage comparator, hold amplifier, and VCMP hold regulator. When the retract is commanded the VCM power driver is tri-stated. The fly back detect circuit keeps the VCM BEMF amplifier disabled until both of the VCM terminals are out of voltage fly back range (above V_{RET5} or below ground). The VCM BEMF differential amplifier then samples the VCM BEMF voltage. The VCM BEMF voltage is transferred to an external apacitor connected between the VBEMF pin 32 and VPARK pin 34. The VCM BEMF timing circuit allows 170 ms for sampling the BEMF before enabling retract.

The park amplifier attenuates the hold voltage by 16 and level shifts it to $V_{RET}/2$. The park amplifier output is available at VPARK pin 16. An external resistor voltage divider across the BEMF sampling capacitor is used to program the retract input control voltage to the VCM power amplifier. The VCM power amplifier retract control voltage is programmed on VPROG pin 33. The programmable retract voltage buffer is enabled after the BEMF sampling delay is expired. The VCM then starts to retract in a voltage controlled closed loop fashion using the sampled BEMF information (VCM velocity when retract is commanded). At the end of the controlled retract phase the voltage across the VCM terminals will equal 16 times the programmed voltage at the VPARK pin 16 (the power amplifier differential gain equal 16). When retract is performed while VCC12 voltage is switched off the retract circuit uses the spindle BEMF voltage as a power supply (V_{RET5} pin 24).

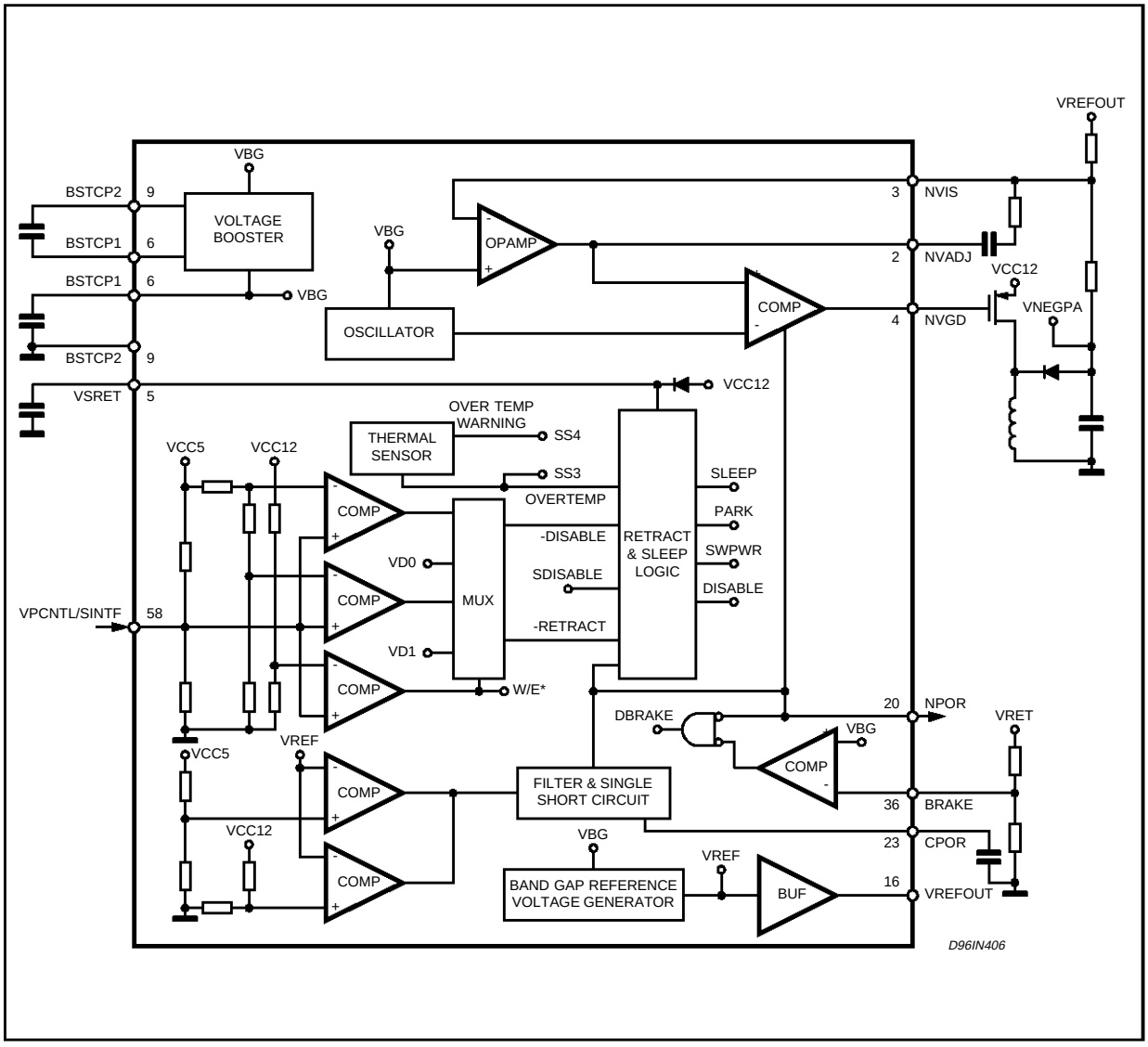
The VCM power amplifier circuit can not function at low V_{RET5} voltage. When the V_{RET5} voltage falls below 4.8 volts the hold comparator trips, switches off the retract circuit and enables the

hold circuit. This condition is latched, and the VCMN terminal is switched to ground while the hold circuit regulator tries to maintain a constant voltage on the VCMP terminal. As long as V_{RET5} voltage is higher than 2 volts the hold circuit regulator will maintain a constant voltage across the VCM terminal this voltage should equal the programmed voltage at VHOLD pin 35.

VCM Driver Offset Comparator

An internal voltage comparator is connected across the VCM power driver output VCMN pin 27 and VCMP pin 22. The comparator output is available on SENVOV (pin 18) when the spindle is programmed to operate in the inductive sense mode. The comparator output is also available in the serial interface mode on bit 5 of the L6254 status register [see REG - 07h STATUSREG: L6254 Status Register (Read Only) on page 20]. The comparator is designed to assist the servo microcontroller in calibrating the VCM driver offset voltage.

Figure 9: L6254 Power Monitor and Negative Voltage Regulator Block Diagram.



POWER MONITOR

Power Monitor Circuit Block Diagram

The power monitor circuit block diagram is shown in Figure 10.

The power monitor comparators monitor the voltage level of both the V_{CC5} pin 11 and the V_{CC12} pin 7. If any voltage falls below the threshold, a current source starts charging an internal capacitor. The capacitor should be charged up to the Schmitt trigger level of 2.5 volts before it can reset the power-on-reset latch. This timing circuit is being used to filter the fast glitches on the power supply lines. Once the power-on-reset condition is cleared if and only if an internal current source could successfully charge an external capacitor at the CPOR pin 23 to the Schmitt trigger level of 2.5 volts. During the power on reset time any glitches on the V_{CC12} and V_{CC5} lines will discharge the external capacitor.

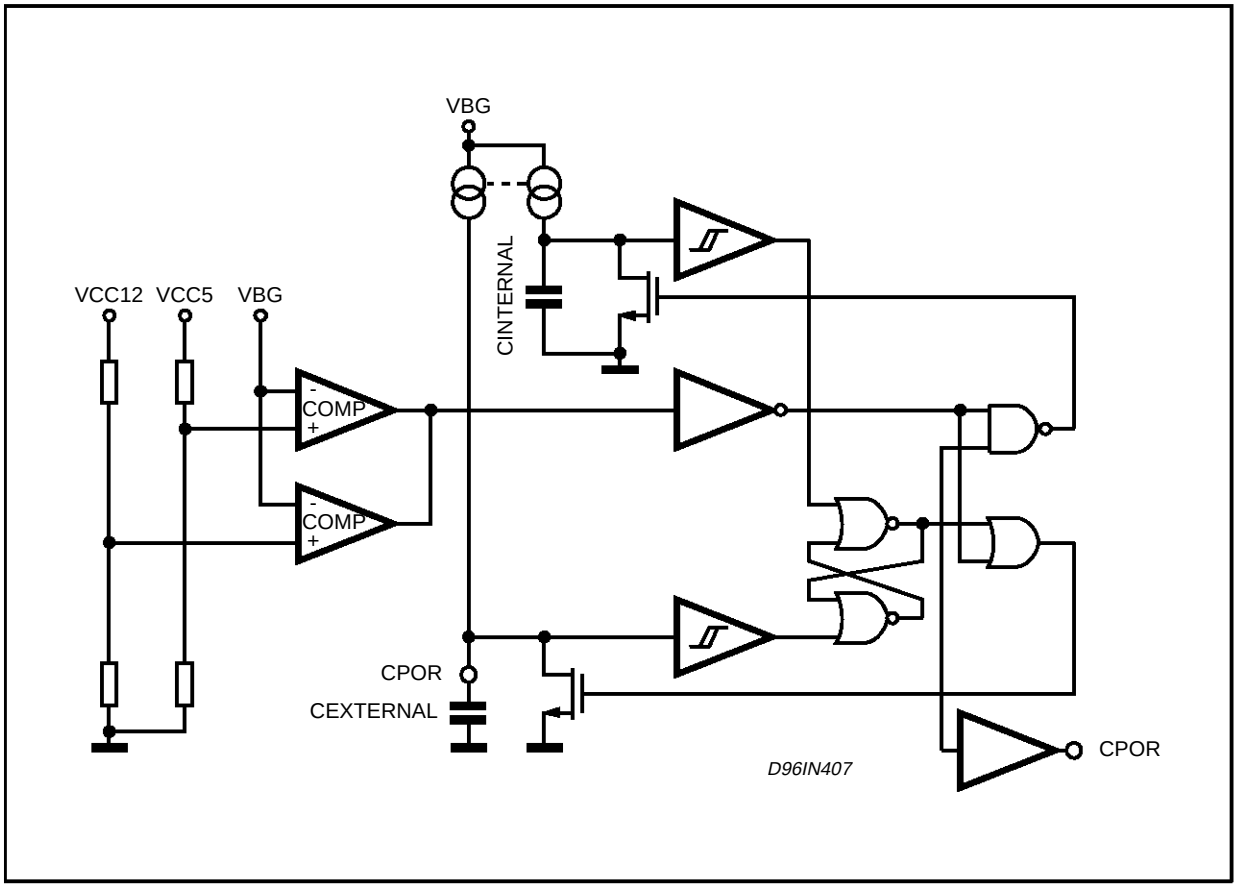
Negative Power Supply Voltage Regulator

The negative voltage regulator consists of a triangular wave oscillator, an error amplifier and a comparator. Review figure 2-6 a complete block diagram of the negative voltage regulator including the external components. The internal error operational amplifier amplifies the difference between the magnitude of the negative voltage value and VREFOUT value. The voltage difference value is realized by two summing resistors which are places externally. The ratio of the two resistors determines the nominal value of the regulated negative voltage. The error amplifier summing junction is available at NVIS pin 3 and the amplifier output is available at NVADJ pin 2. The voltage error gain and the regulator voltage feedback loop dynamic compensation can be adjusted by the external components across these two pins.

A voltage clamp is placed on the error amplifier output to ensure current in the inductor during start up.

A voltage comparator compares the output of the error amplifier to an internal triangular wave oscillator output and generates a constant frequency variable duty cycle signal. The output of the comparator is available at NVGD pin 4. The comparator drives the gate of an external PMOS power transistor switch. The nominal value of the triangular wave oscillator frequency is 260 KHz. The external switch charges an external inductor. The voltage on the inductor is transferred to a capacitor using a diode in a voltage inverter configuration. Both the diode and the capacitor are places

Figure 10: L6254 Power Monitor Block Diagram.



externally to avoid any negative voltage on the L6254 IC pins. Under normal specified load conditions and correct scaling of the external components the regulator circuit should operates in a constant frequency variable duty cycle switch mode without any cycle slips. Refer to the theory of operation section 7 for scaling the external components and the electrical specification section 6 for the negative voltage regulator internal components specification.

The regulator is disabled during power on reset.

Over Temperature Protection

The L6254 temperature protection circuit consists of a temperature sense circuit and two voltage comparators. The temperature sense circuit generates a voltage proportional to the absolute die temperature. A voltage comparator monitors this voltage and trips when the die temperature exceeds 140°C. The comparator output signal indicates a temperature warning condition. The temperature warning signal is only available in the L6254 serial interface configuration and can be read from the status bit 3 in the L6254 status register address 7. An additional comparator monitors the temperature and trips when the die temperature exceeds 160°C. This comparator output indicates an over temperature condition and automatically drives the L6254 IC into sleep mode. The over temperature status is only available in the serial interface configuration and can be read from the status bit 4 in the L6254 status register address 7. A 25°C hysteresis is places on this comparator to allow the die temperature to stabilize before enabling the L6254 IC.

THEORY OF OPERATION

Figure 11: L6254 Spindle Linear Transconductance Loop Application Circuit.

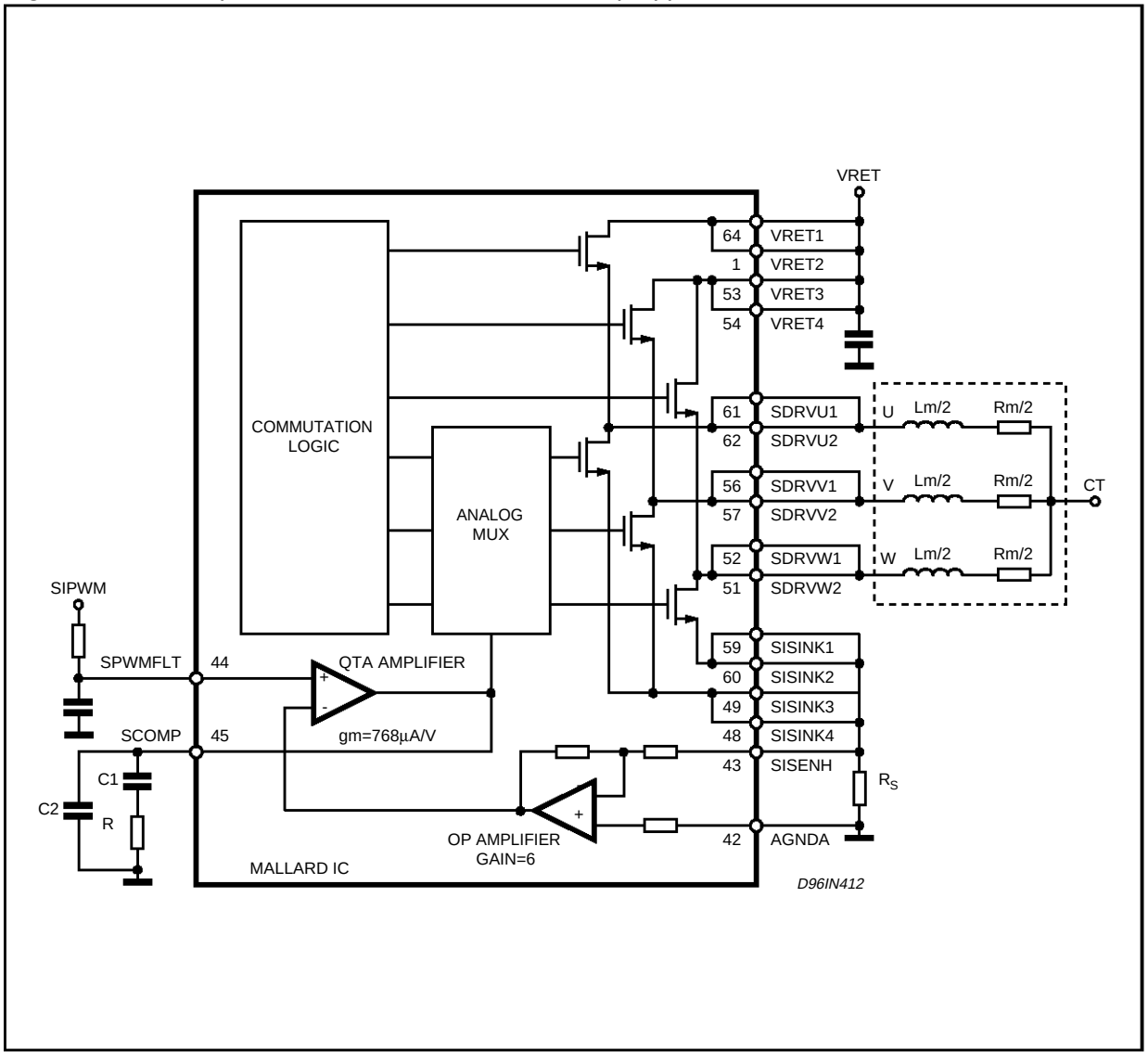
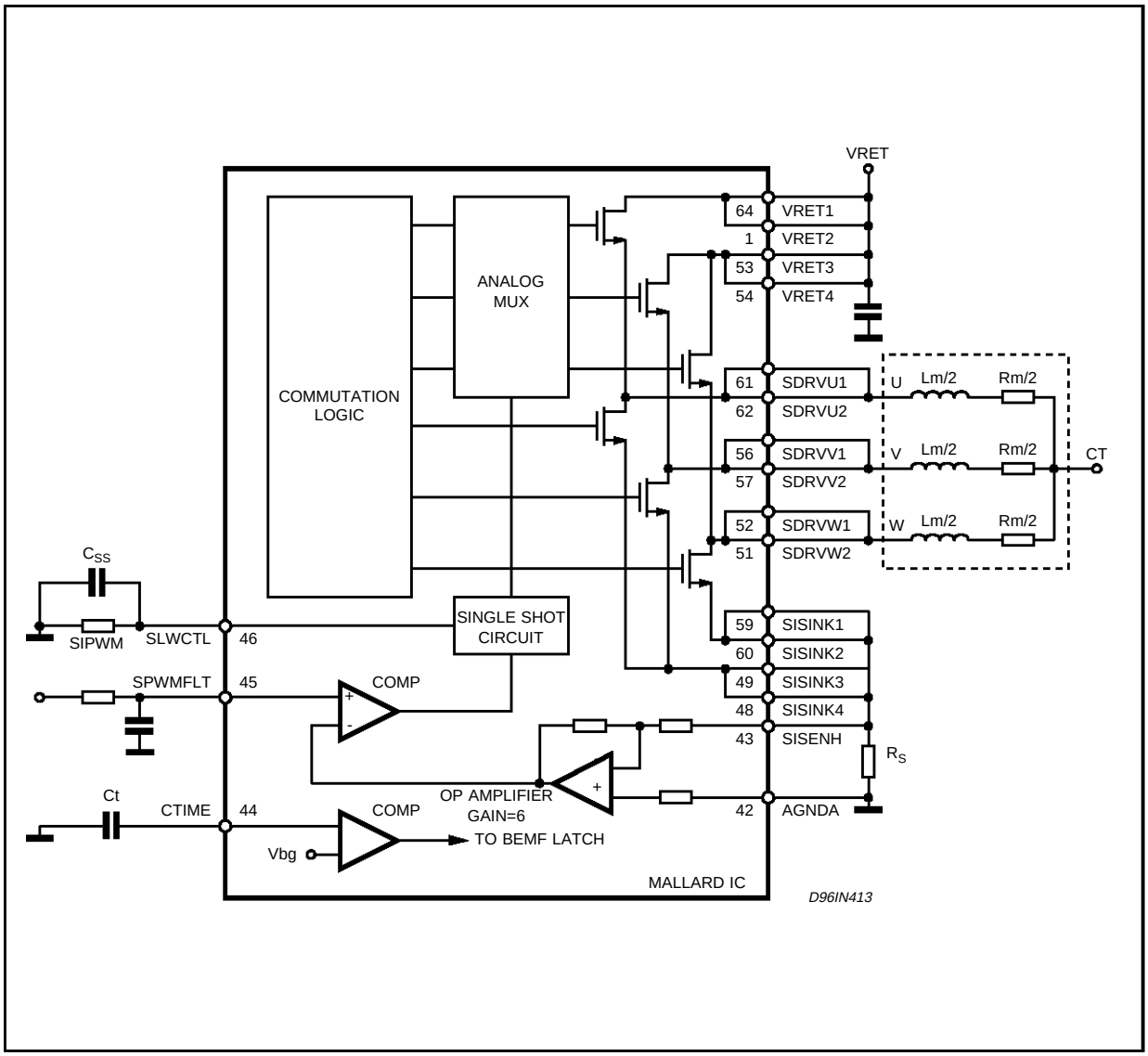


Figure 12: L6254 Spindle Switch Mode Control Loop Application Circuit.



VCM TRANSCONDUCTANCE LOOP DESIGN

A block diagram of the VCM transconductance loop application circuit is shown in Figure 13. The VCM input current request is commanded from the microcontroller to the drive ASIC two bit PWM DAC. The DAC output is filtered using a third order Butterworth filter. The filtered VCM current is available at the L6254 sallen Key filter buffer output VFLTM pin 40. The filter current command is the level shifted to VRET/2 and the output of the level shifter is VFLTOUT pin 41. At zero input current request the output at VFLTM should be scaled to $V_{REF}/2$ then the output of the level shifter at VFLTOUT will equal to $V_{RET5}/2$.

It is recommended to scale the dynamic range of the velocity command at VFLTM to +/-1 volts to utilize the best response of the sallen key buffer amplifier, however the amplifier dynamic range buffer can support up to +/-4 volts signal swing.

The open loop transfer function of the VCM transconductance loop from VFILTOUT pin 41 to VISENS1 pin 31 can be calculated using the block diagram in Figure 13.

TF = Ger x Gpa x Gm x Gs

Where,

TF	VCM transconductance open loop transfer function [V/V]
Ger	Error amplifier gain [V/V]
Gpa	Power amplifier gain differential gain [V/V]
Gm	Motor transfer function [V/V]
Gs	Current sense amplifier gain [V/V]

Ger Calculation

We assume the amplifier is operating in the linear range inside the clamp window. The clamp window is approximately +/-1.8 volts around $V_{RET}/2$.

If we normalize the gain for VISENS1 and VFLTOUT summing resistor ratio R1/R2.

The error amplifier normalized gain equals;

$\rightarrow$ Ger = [(R1/R2) (1 + j W (C R3)] / (j W C R1)

GpA Calculation

The power amplifier unity gain bandwidth is 2 Mhz. We then consider the amplifier to have a flat response in our frequency range of interest. The amplifier consists of an inverting and noninverting gain stage driving deferentially a two phase power bridge in a follower configuration. Ignoring the amplifier secondary effects, the differential gain of the power amplifier equals;

$\rightarrow$ Gpa = 16

Gm Calculation

Ignoring the effect of the VCM BEMF, contacts & cabling stray reactance and motor eddy current losses. The motor transfer function equals;

$\rightarrow$ Gm = (Rs/[Rm + Rs]) / (j W [Lm/ (Rm + Rs)] + 1)

Gs Calculation

The current sense amplifier unity gain bandwidth is 2 Mhz. We then consider the amplifier to have a flat response in our frequency range of interest.

$\rightarrow$ Gs = 8

The VCM transconductance open loop transfer function will take the form:

TF = [Go (1 + j W (C R3))] / [(1 + j W [Lm / (Rm + + Rs)) (j W)]

Where;

Go DC open loop gain = (128 Rs) / (C R2 [Rm + Rs])

The transconductance loop is a first order loop. The simplest loop compensation is to select the lead term of th error amplifier to be equal to the motor time constant.

From that;

CR3 = Lm / (Rm + Rs)

then the open loop transfer function will reduce to;

TF = Go/j W

The VCM transconductance closed loop bandwidth will equal to the open loop gain Go

Numerical example:

Lm = 1 mH

Rm = 10 ohms

Rs = 0.33 ohms

Maximum command current = +/- 1.25 Ampere

Desired VCM transconductance closed loop bandwidth = 20 Khz

1 - Calculate R1 and R2

Assume that VFLTOUT swing at +/-1.25 A = 1volt

[Recommended for amplifier ac performance]

VISENS1 swing at +/- 1.25 A = 0.33 x 8 x 1.25 = 3.3V

Then R1/R2 ratio = 3.3

Select R2 = 10 K then R1 = 33 K

[Amplifiers maximum output current (swing/R1) mA]

2 - Calculate C

Go = Wo = (128 Rs) / (C R2 [Rm + Rs])

C = (128 Rs) / Wo R2 [Rm + Rs])

C = 3.254 E-9 select 3.3 nF

3 - Calculate R3

R3 = Lm / [C(Rm + Rs)]

= 2.93 E4 select 29.7 Kohm

Figure 13: VCM Transconductance Loop Application Circuit.

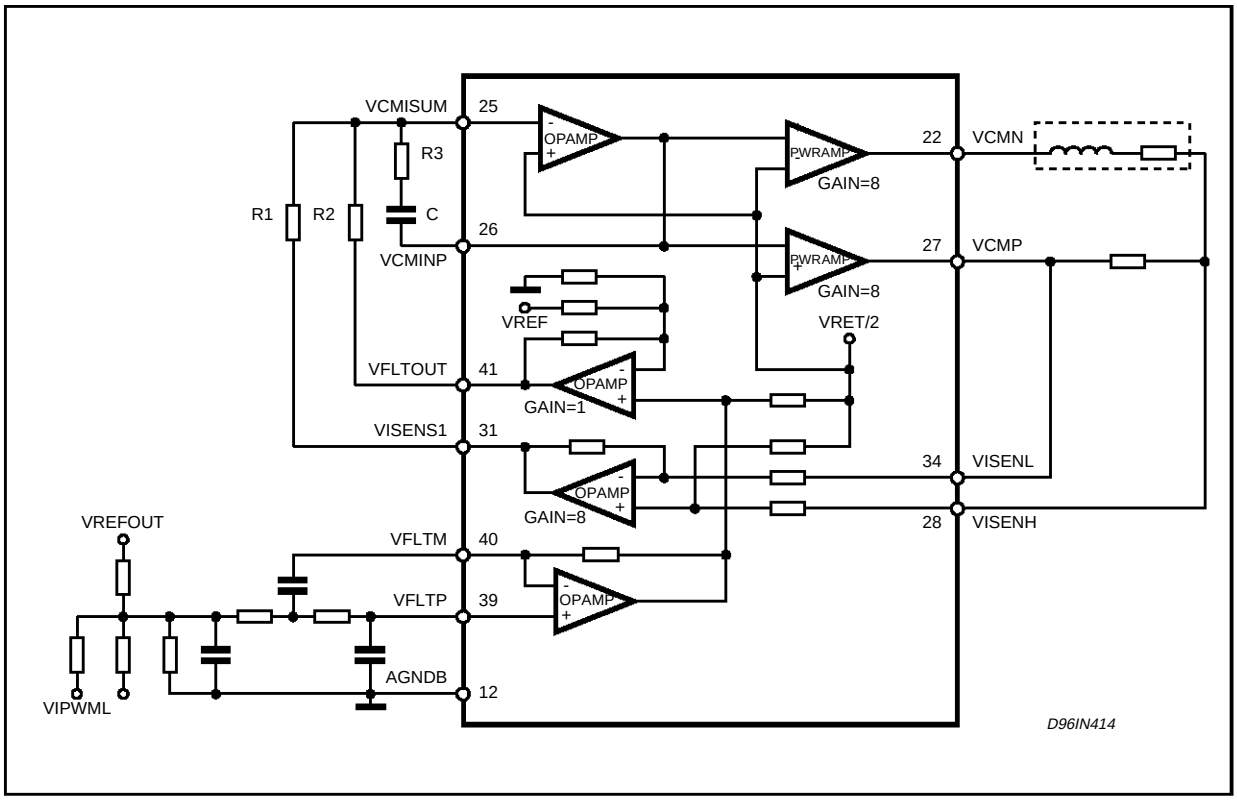
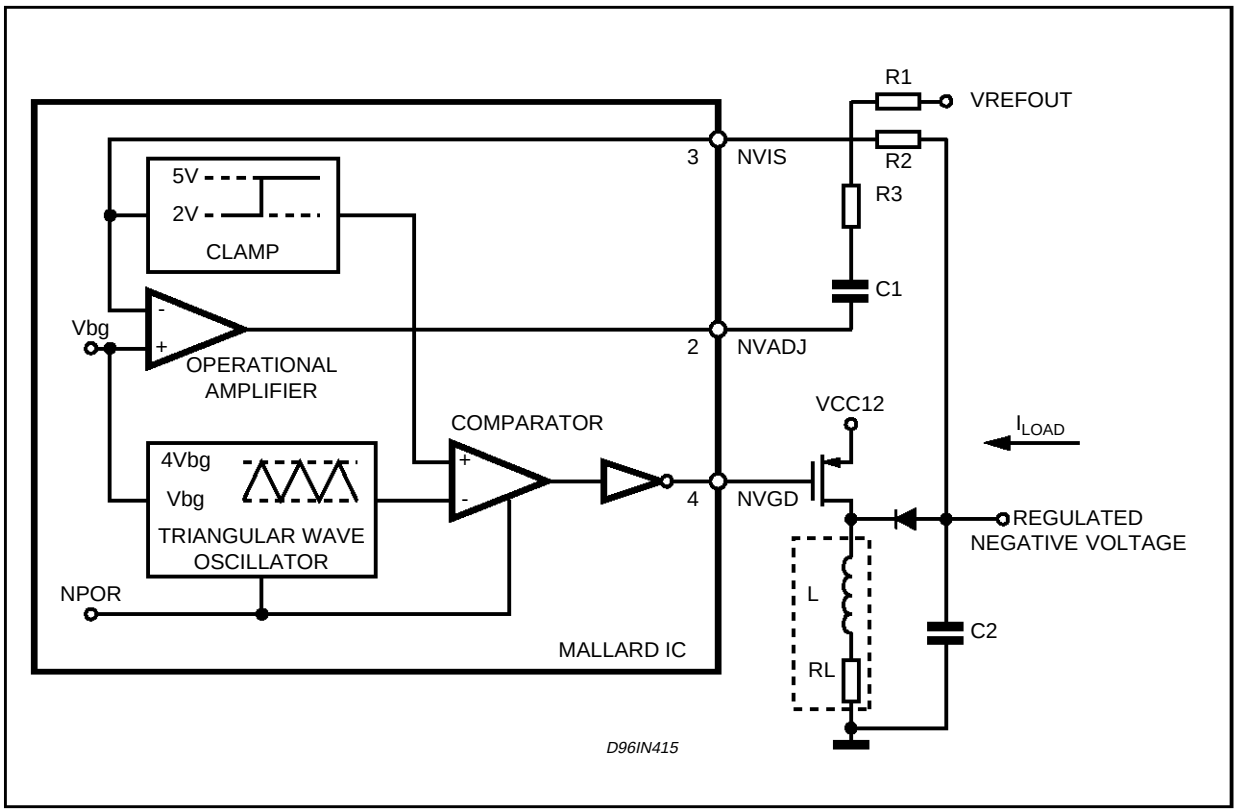


Figure 14: Negative Voltage Regulator Application Circuit.



THERMAL DATA

Figure 15: High Power & High Resistance Profile

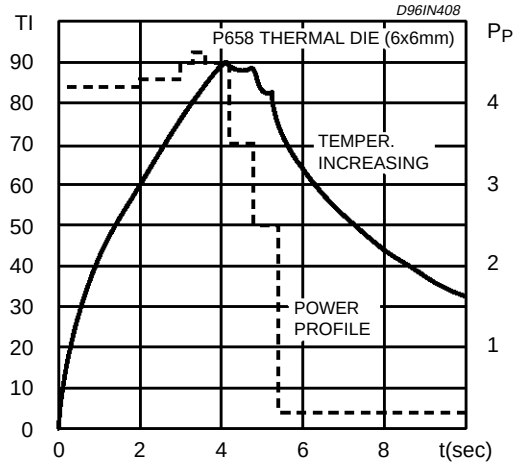


Figure 16: Low Power & High Resistance Profile

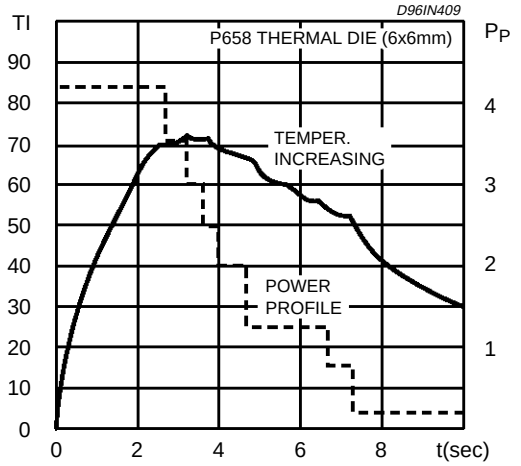


Figure 17: Three Initial Pulses

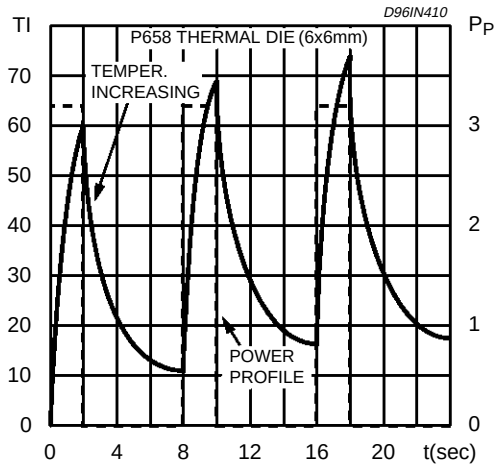
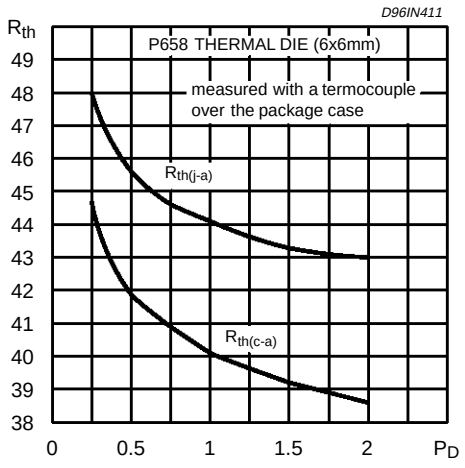


Figure 18: θj-a and θc-a on Test Board



TQFP64 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.18	0.23	0.28	0.007	0.009	0.011
C	0.12	0.16	0.20	0.0047	0.0063	0.0079
D		12.00			0.472	
D1		10.00			0.394	
D3		7.50			0.295	
e		0.50			0.0197	
E		12.00			0.472	
E1		10.00			0.394	
E3		7.50			0.295	
L	0.40	0.60	0.75	0.0157	0.0236	0.0295
L1		1.00			0.0393	
K	0°(min.), 7°(max.)